REMARKS

The Office Action mailed May 20, 2002, has been received and reviewed. Claims 1 through 40 are currently pending in the application. Claims 1 through 40 stand rejected.

Reconsideration of the above-referenced application is respectfully requested.

Information Disclosure Statement

Please note that a Supplemental Information Disclosure Statement was filed herein on November 21, 2001, and that no copy of the PTO-1449 was returned with the outstanding Office Action. Applicants respectfully request that the information cited on the PTO-1449, which is the same as that of record to that date in the parent application hereto, be made of record herein. For the sake of convenience, a second copy of the November 21, 2001, Supplemental Information Disclosure Statement, PTO-1449, and USPTO date-stamped postcard are enclosed herewith. It is respectfully requested that an initialed copy of the PTO-1449 evidencing consideration of the cited references be returned to the undersigned attorney.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,477,082 to Buckley, III et al.

Claims 1, 2, 4-10, 14-29, and 33-39 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Buckley, III et al., U.S. Patent No. 5,477,082.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

It is respectfully submitted that Buckley fails to expressly or inherently describe each and every element as set forth in claims 1, 2, 4-10, 14-29, and 33-39.

Buckley discloses a method for interconnecting at least two semiconductor dice. However, unlike Applicants' method, the dice in Buckley contact through an intervening carrier which carries all of the electrically conductive elements that electrically connect bond pads of the at least two semiconductor dice to each other. Col. 2, lines 29-32. The carrier requirement dictates that the electrically conductive elements that join the die which is above the carrier to the die which is below be physically bridged by the carrier.

In contrast, amended claim 1 recites that the conductive structures are laterally discrete and physically unconnected from each other. Such a requirement excludes the use of an intermediate carrier.

As Buckley does not expressly or inherently describe each and every element of amended claim 1, it is respectfully submitted that, under 35 U.S.C. § 102(b), amended claim 1 is allowable over Buckley.

Claims 2, 4-10, and 14-22 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 4 is additionally allowable since Buckley lacks any express or inherent description of a method within the scope of amended claim 1 and in which electrically connecting bond pads of a first and at least one second semiconductor dice includes providing conductive structures between *each of* a plurality of bond pads of the at least one second semiconductor die and corresponding bond pads of the first semiconductor die.

In claim 9, a distinction is made between the bond pads by which the first semiconductor die is electrically connected to the at least one second semiconductor die and the bond pads by which the first die is electrically connected to the carrier (*i.e.*, the "other" bond pads). Claim 8, from which claim 9 depends, recites that these *other* bond pads "remain exposed beyond an outer periphery of [the] at least one second semiconductor die." As shown and described in Buckley, no semiconductor die includes some bond pads that are electrically connected to bond pads of another semiconductor die and *other* bond pads which are exposed beyond the outer periphery of the other semiconductor die *and* electrically connected to a carrier.

Claim 19 is additionally allowable since Buckley neither expressly nor inherently describes securing a first member of a conductive element, which is secured to each other bond pad, and a second member of the conductive element, which is secured to a contact pad of a carrier substrate, *directly* to one another.

Independent claim 23, as amended and presented herein, recites a method for packaging a semiconductor device assembly which includes, among other things, electrically connecting bond pads of a first semiconductor die and corresponding bond pads of a second semiconductor die with "laterally discrete, physically disconnected conductive structures."

Buckley does not expressly or inherently describe a semiconductor device packaging method which includes electrically connecting bond pads of two semiconductor devices with laterally discrete, physically disconnected conductive structures. Instead, the description of Buckley is limited to the use of substrates that carry conductive vias and traces to connect corresponding bond pads of two or more semiconductor devices. The substrates described in Buckley physically connect these conductive structures and are configured to be interposed between the semiconductor devices.

Each of claims 24-29 and 33-38 is allowable, among other reasons, as depending either directly or indirectly from claim 23, which is allowable.

Claim 25 is additionally allowable since Buckley lacks any express or inherent description of "electrically connecting bond pads of [a] first semiconductor die exposed beyond an outer periphery of . . . at least one second semiconductor die to . . . corresponding contacts of [a] carrier."

Claim 35 is further allowable because Buckley neither teaches nor suggests securing first and second members of conductive elements directly to each other.

Independent claim 39, as amended and presented herein, recites a method for packaging a semiconductor device assembly that includes a first semiconductor die and at least one second semiconductor die with active surfaces thereof facing one another. The method of amended

claim 39 also includes, among other things, electrically connecting at least some bond pads of the at least one second semiconductor die with corresponding bond pads of the first semiconductor die via laterally discrete, physically disconnected conductive structures.

Again, Buckley lacks any express or inherent description of the use of laterally discrete, physically disconnected conductive structures to electrically connect bond pads of two or more semiconductor dice that face one another.

As such, Buckley fails to anticipate each and every element of amended claim 39 and amended claim 39 is, therefore, allowable over Buckley under 35 U.S.C. § 102(b).

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,477,082 to Buckley, III et al.

Claims 3, 11-13, 30-32 and 40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Buckley. In addition, claims 11, 12, 30 and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Buckley as applied to claims 10 and 29 above, and further in view of Maurinus (U.S. Patent No. 5,302,778).

Claims 3, and 11-13 are allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

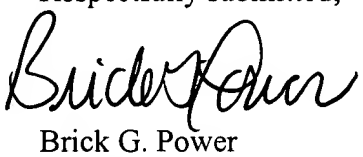
Claims 30-32 are allowable, among other reasons, as depending from claim 23, which is allowable.

Claim 40 has been amended to alleviate ambiguous wording. Amended claim 40 recites a *second* multi-chip module attached to the same carrier as in Claim 39. Claim 40 is allowable, among other reasons, as depending from claim 39, which is allowable.

CONCLUSION

Claims 1-40 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Twice amended) A method for interconnecting at least two semiconductor dice, comprising:

providing a first semiconductor die including a plurality of bond pads arranged in an array over an active surface thereof;

providing at least one second semiconductor die including a plurality of bond pads on an active surface thereof;

orienting said first semiconductor die and said at least one second semiconductor die with said active surfaces thereof facing each other;

electrically connecting at least some bond pads of said plurality of bond pads of said at least one second semiconductor die with corresponding bond pads of said plurality of bond pads of said first semiconductor die <u>via laterally discrete, physically unconnected conductive structures</u>.

4. (Amended) The method of claim 1, wherein said electrically connecting comprises providing conductive structures directly between <u>each of</u> said plurality of bond pads of said at least one second semiconductor die and said corresponding bond pads of said first semiconductor die.

6. (Amended) The method of claim 4, wherein said providing conductive structures comprises providing structures formed from a material comprising at least one of a metal, an alloy, a conductive epoxy, <u>and</u> a conductor-filled epoxy[, and a z-axis conductive elastomer].

16. (Twice amended) The method of claim 14, wherein said disposing said conductive elements between said other bond pads of said first semiconductor die and said corresponding contacts of said carrier comprises providing a quantity of a material comprising at least one of a metal, an alloy, a conductive epoxy, <u>and</u> a conductor-filled epoxy[, and a z-axis conductive elastomer].

19. (Amended) The method of claim 18, further comprising securing at least said first and second members of said conductive element directly to each other.

23. (Amended) A method for packaging a semiconductor device assembly, comprising:

providing a first semiconductor die including a plurality of bond pads arranged in an array over an active surface thereof;

providing at least one second semiconductor die including a plurality of bond pads arranged on an active surface thereof;

orienting said at least one second semiconductor die over said first semiconductor die with said active surface facing said active surface of said first semiconductor die, said plurality of bond pads of said at least one second semiconductor die in alignment with corresponding bond pads of said first semiconductor die;

electrically connecting at least some bond pads of said plurality of bond pads of said at least one second semiconductor die with corresponding bond pads of said plurality of bond pads of said first semiconductor die via laterally discrete, physically unconnected conductive structures;

providing a carrier with a plurality of contacts; and

orienting said first semiconductor die over said carrier with said active surface facing said carrier, bond pads of said first semiconductor die exposed beyond an outer periphery of said at least one second semiconductor die in alignment with corresponding contacts of said carrier.

35. (Twice amended) The method of claim 34, further comprising securing at least said first and second members of said conductive element directly to each other.

39. (Amended) A method for packaging a semiconductor device assembly, comprising:

providing at least a first multi-chip module including:

a first semiconductor die with a plurality of bond pads arranged in an array over an active surface thereof; and

at least one second semiconductor die including a plurality of bond pads arranged on an active surface thereof, each of said plurality of bond pads of said at least one second semiconductor die in alignment with corresponding bond pads of said first semiconductor die, said active surfaces of said first semiconductor die and said at least one second semiconductor die facing one another, and said bond pads of said at least one second semiconductor die electrically connected to said corresponding bond pads of said first semiconductor die, other bond pads of said first semiconductor die exposed laterally beyond an outer periphery of said at least one second semiconductor die;

electrically connecting at least some bond pads of said plurality of bond pads of said at least one second semiconductor die with corresponding bond pads of said plurality of bond pads of said first semiconductor die via laterally discrete, mutually disconnected conductive elements;

providing a carrier including contacts; and

orienting said at least said first multi-chip module over said carrier with said active surface of said first semiconductor die facing said carrier and said other bond pads in alignment with corresponding contacts of said carrier.

40. (Amended) The method of claim 39 further comprising:

providing at least a second multi-chip module including:

[a] another first semiconductor die with a plurality of bond pads arranged in an array over an active surface thereof; and

an another at least one second semiconductor die including a plurality of bond pads arranged on an active surface thereof; each of said plurality of bond pads of said another at least one second semiconductor die in alignment with corresponding

bond pads of said another first semiconductor die, said active surfaces of said another first semiconductor die and said another at least one second semiconductor die facing one another, and said bond pads of said another at least one second semiconductor die electrically connected to said corresponding bond pads of said another first semiconductor die, other bond pads of said another first semiconductor die exposed laterally beyond an outer periphery of said another at least one second semiconductor die; and

orienting said another at least said second multi-chip module over said carrier with said active surface of said another first semiconductor die facing said carrier and said other bond pads in alignment with corresponding contacts of said carrier.